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Forschungsfabrik Mikroelektronik Deutschland

The APECS pilot line is powering the evolution of chiplet technologies

Fraunhofer Group for Microelectronics in cooperation with the Leibniz Institutes FBH and IHP

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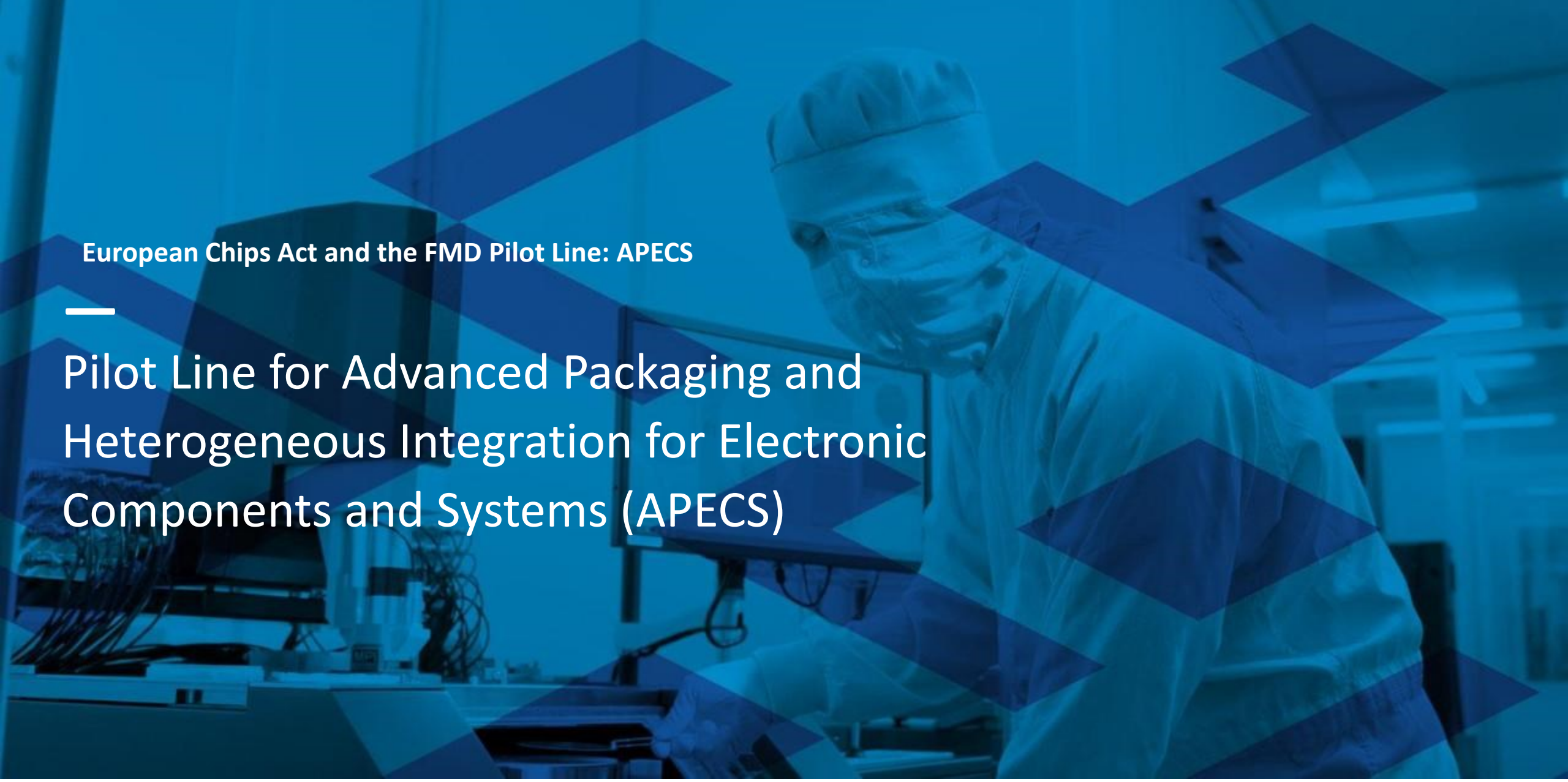

European Chips Act and the FMD Pilot Line: APECS

Pilot Line for Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems (APECS)

EU Chips Act, Nov. 30th 2023

Implementation via 3 Pillars

Pillar 1

»Chips for Europe Initiative«
Strengthening research, development and innovation

Pillar 2

»Security of Supply«
Support for new types of production facilities and EU foundries

Pillar 3

»Monitoring and Crisis Response«
Coordination mechanism for monitoring the supply of semiconductors

*Source: European Commission, Eurpean Parliament, Statista European Union, 2022

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Pan European Pilot Line Facility: Categorization of Pilot Lines

On Definition of RTO Pilot Line vs. Industrial Pilot Line

Leverage on increase of production capabilities

Transfer/Scale-up

RTOs Pilot Lines „Innovation Push“ – ‚Best in Class‘		Industrial Pilot Lines „Scale Up“
Exploratory Services (lower TRLs)	Small Scale Production (mid to high TRLs)	First Industrial Deployment (highest TRLs)
Delivery of Prototypes ▪ Basic architectures and feasibilities for products at an early stage (e.g. for proof-of-concept) ▪ Processes are far from final maturity ▪ PDK* drafted, initial models in place	Delivery of small volume ▪ Technology and Processes can already be used for prototypes and products ▪ Technology frozen, customer specific adaptations possible ▪ PDK* available ▪ Small scale production capacity available (industrial grade)	First delivery of qualified Products ▪ Technology, Processes and Production Methodology under evaluation ▪ Up-scaling of a R&D project ▪ Yield still to be improved, thus, no competitive production possible yet ▪ PDK* finalized

APECS delivers technologies, chips and solutions for next generations of applications in communication, sensing, power, quantum computing, etc.

RTOs Research

Industry Production

* **PDK**: process design kit, model of the fabrication process to be used for the **chip design**

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The APECS pilot line – European chiplet innovation

How APECS leads the way in heterogeneous integration by providing diverse design capabilities, technologies and testing strategies for electronic components and systems on a single platform

FMD Pilot Line APECS

Working Packages

Design Flows

System Design

- STCO Design for 2.5D / 3D
- STCO Design for QMI
- Foundational Chiplets

STCO = System Technology Co-Optimization
QMI = Quasi-monolithic integration

Interface Processing: Chiplet integration

Hetero-integration into (quasi-)monolithic integration (QMI)

Chiplet Integration platform (2.5D and 3D)

Front End Integration:

- RF Integration
- Photonic Integration
- QMI-Systems

HF = High frequency
QMI = Quasi-monolithic integration

Back End Integration:

- Advanced Packaging
- Functional Integration
- Functional Interposer

Analysis & Metrology

Character., Test & Reliability

- Characterization
- Reliability
- Test

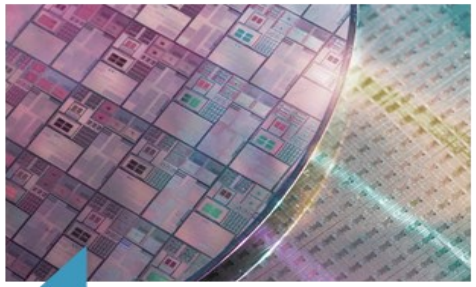
Demos & Application Solutions

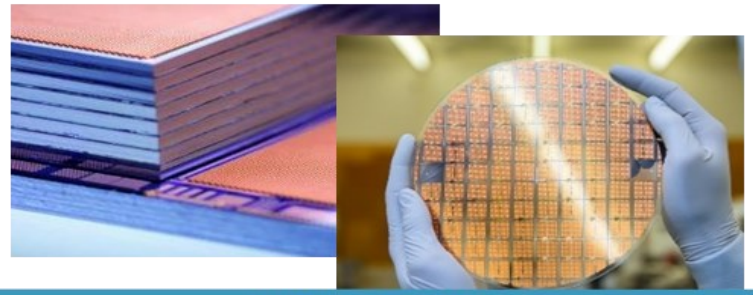
One-Stop-Shop

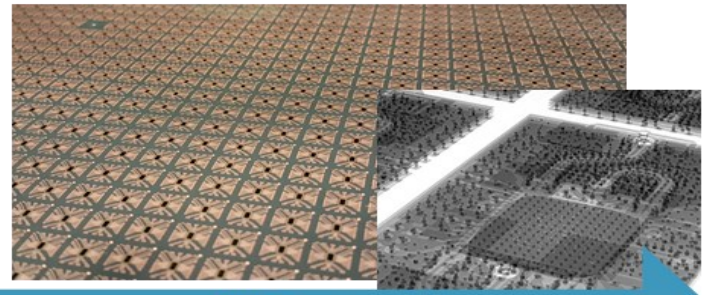
Fraunhofer IZM – Merging of Wafer- and Panel-Level Technologies

Fraunhofer – Heterogeneous Integration

From Wafer Level System Integration to Panel Level System Integration







CMOS Feature Sizes
5 nm … >100 nm

WLP Feature Sizes
0.75 µm … >10 µm

PLP Feature Sizes
< 5 µm … 100 µm

Wafer Level Packaging (WLP)

Technology: Based on thin film materials & equipment
Wafer size: 100 mm … up to 300 mm
Input: CMOS - III/V - WBG wafers
Output: 2.5D/3D integrated systems or system components

Panel Level Packaging (PLP)

Technology: Based on PCB materials & equipment
Panel size: up to 610 x 456 mm²
Input: CMOS / III/V / wide bandgap dies (w/ bumping)
Output: Packaged/embedded modules

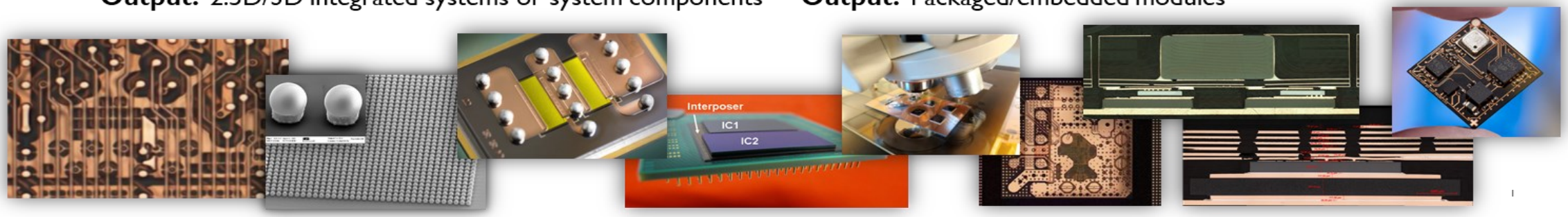
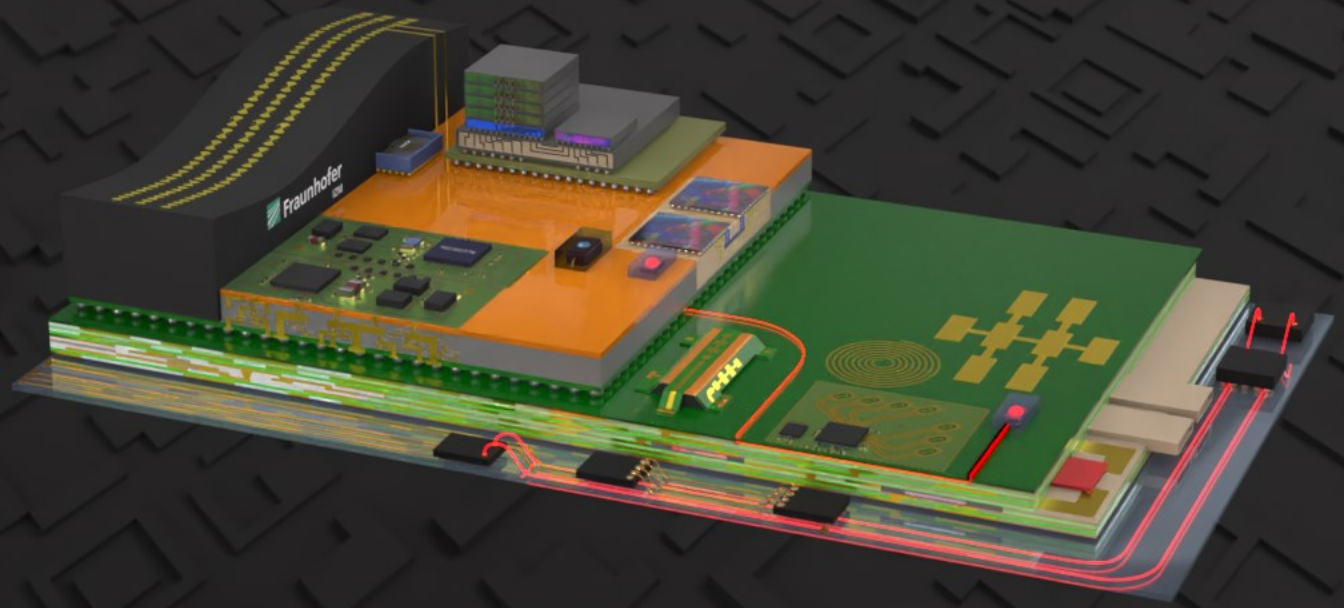


Illustration of possibilities and the complexity of advanced heterogeneous system integration and advanced packaging



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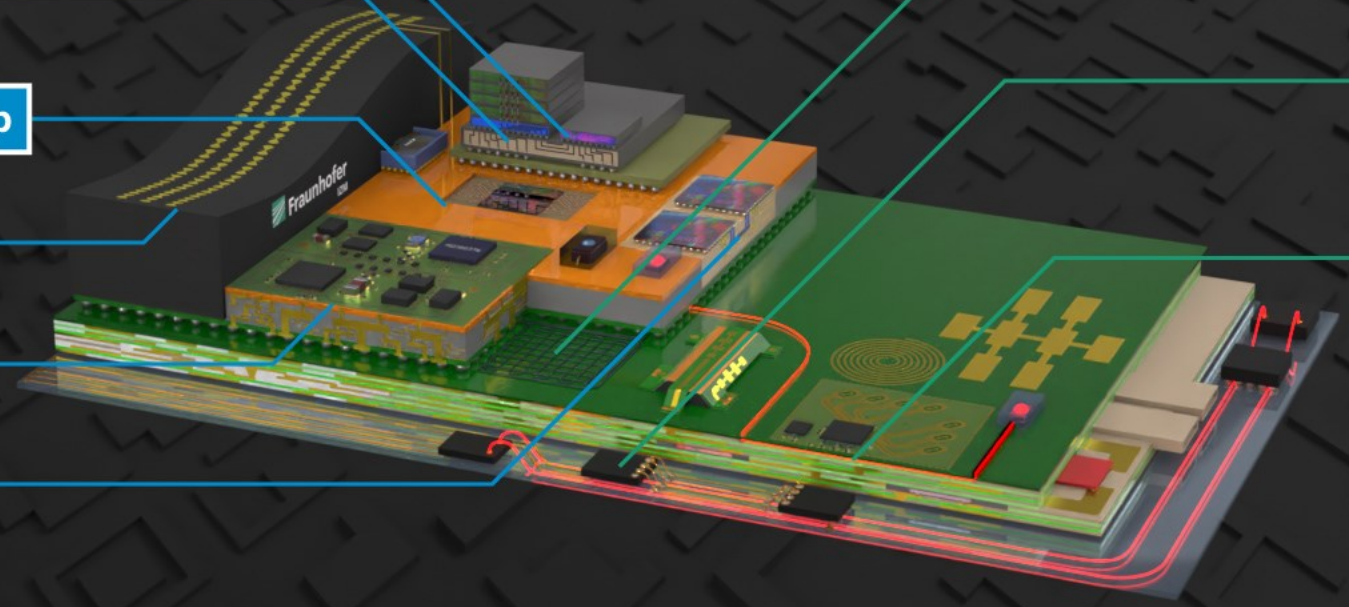
Examples for the integration at wafer and substrate level

Integration at wafer level

- Hybrid Cu/Cu bonds
- HDML Si-Interposer
- TF-embedded thin chip
- 3D-shaped mold cap
- TSV/TGV/TPV
- Embedded Si-bridge



Integration at substrate level

- Metallic TF-on-organic anti-tampering structures
- Embedded passives, chips or SiP module
- Embedded optical waveguides

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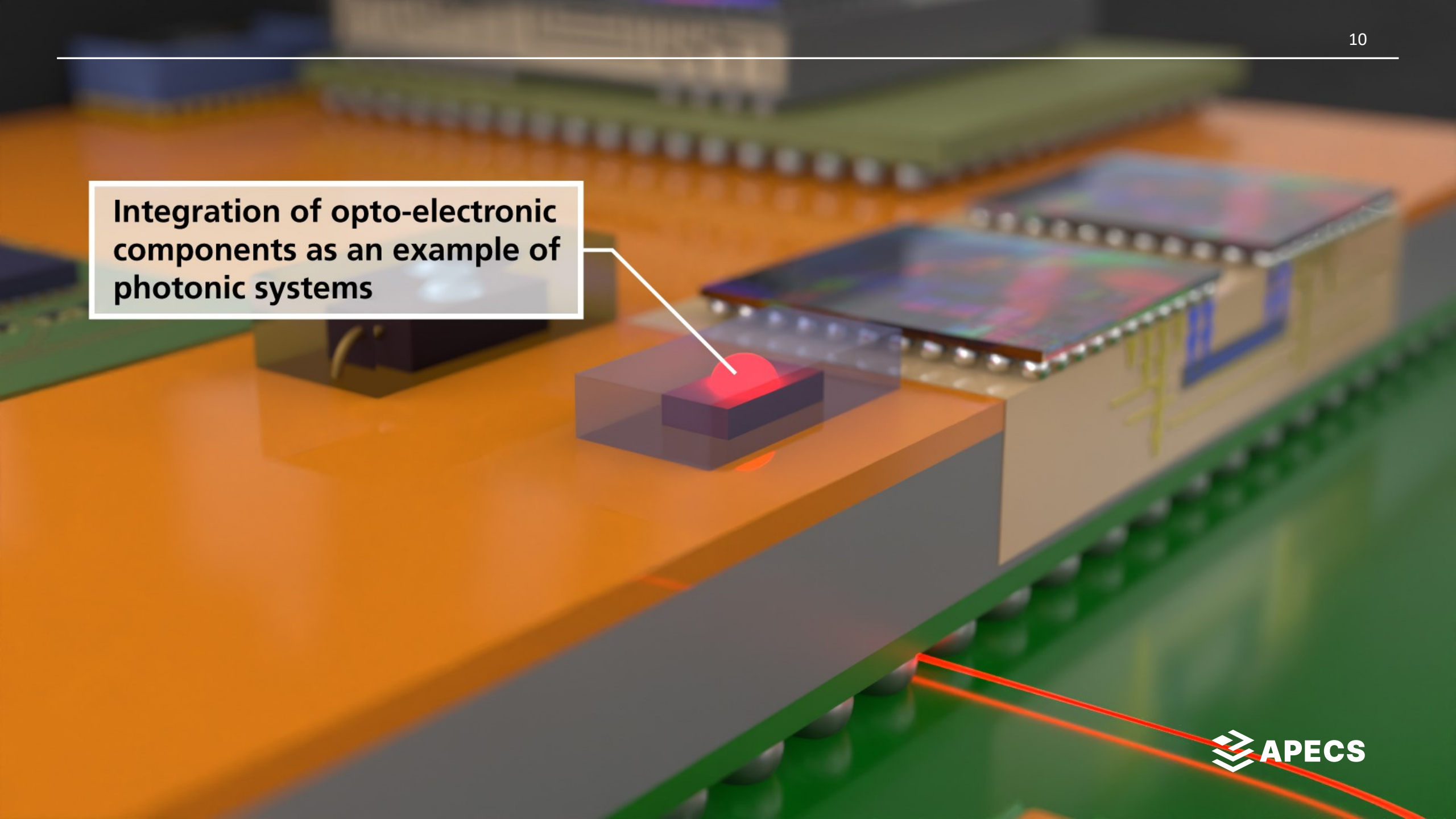
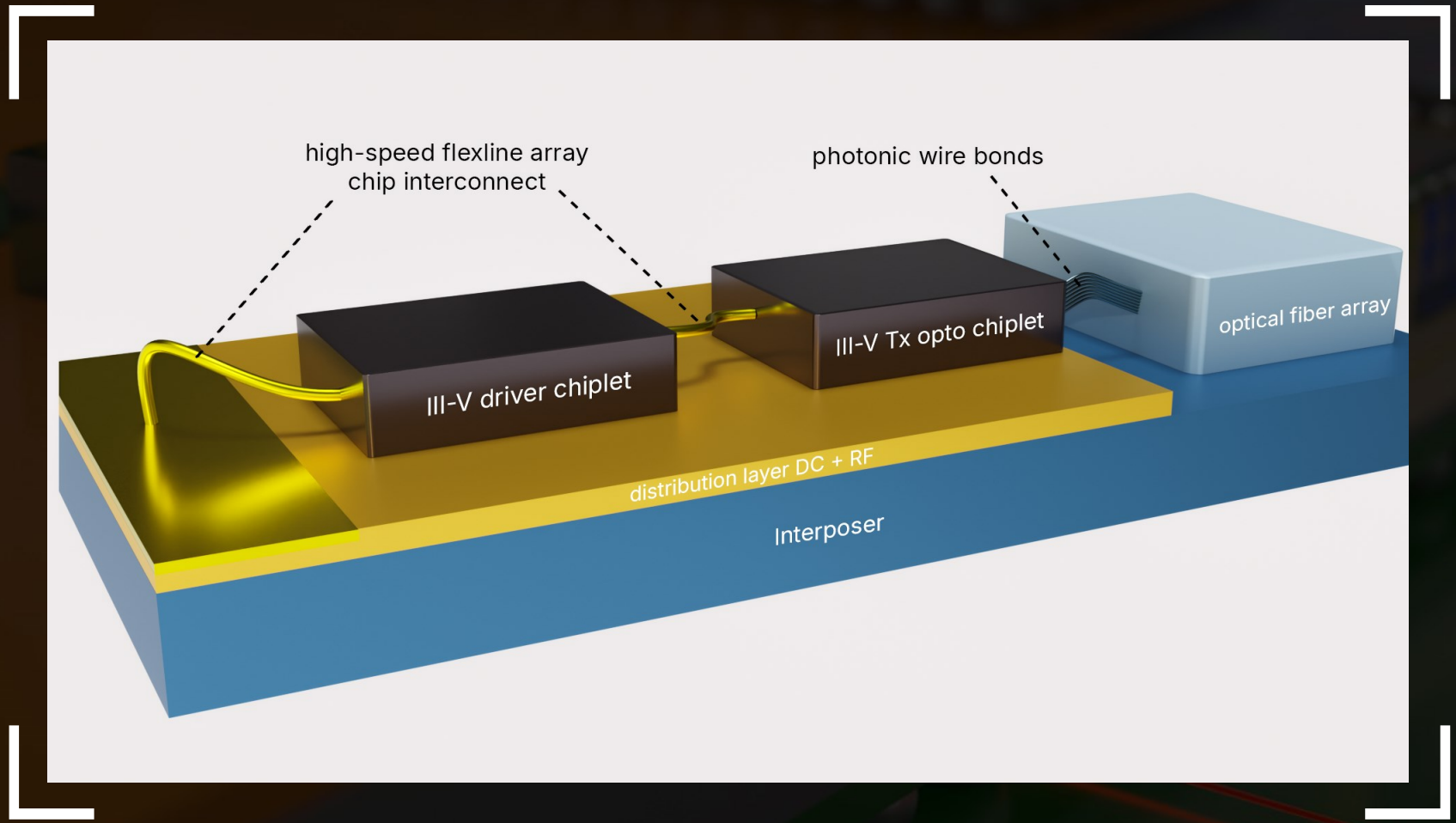

Integration of opto-electronic components as an example of photonic systems

Opto Demonstrator



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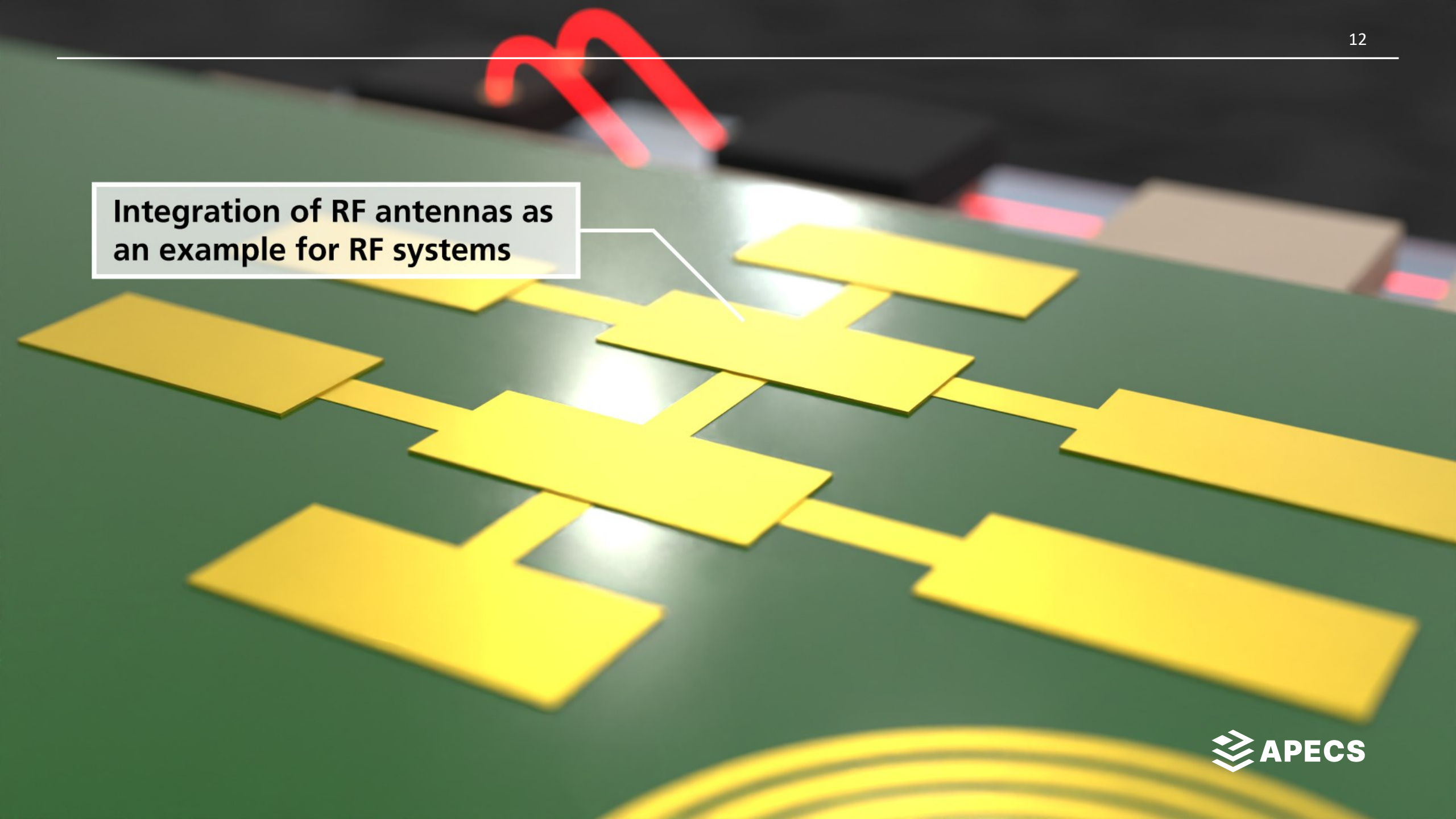
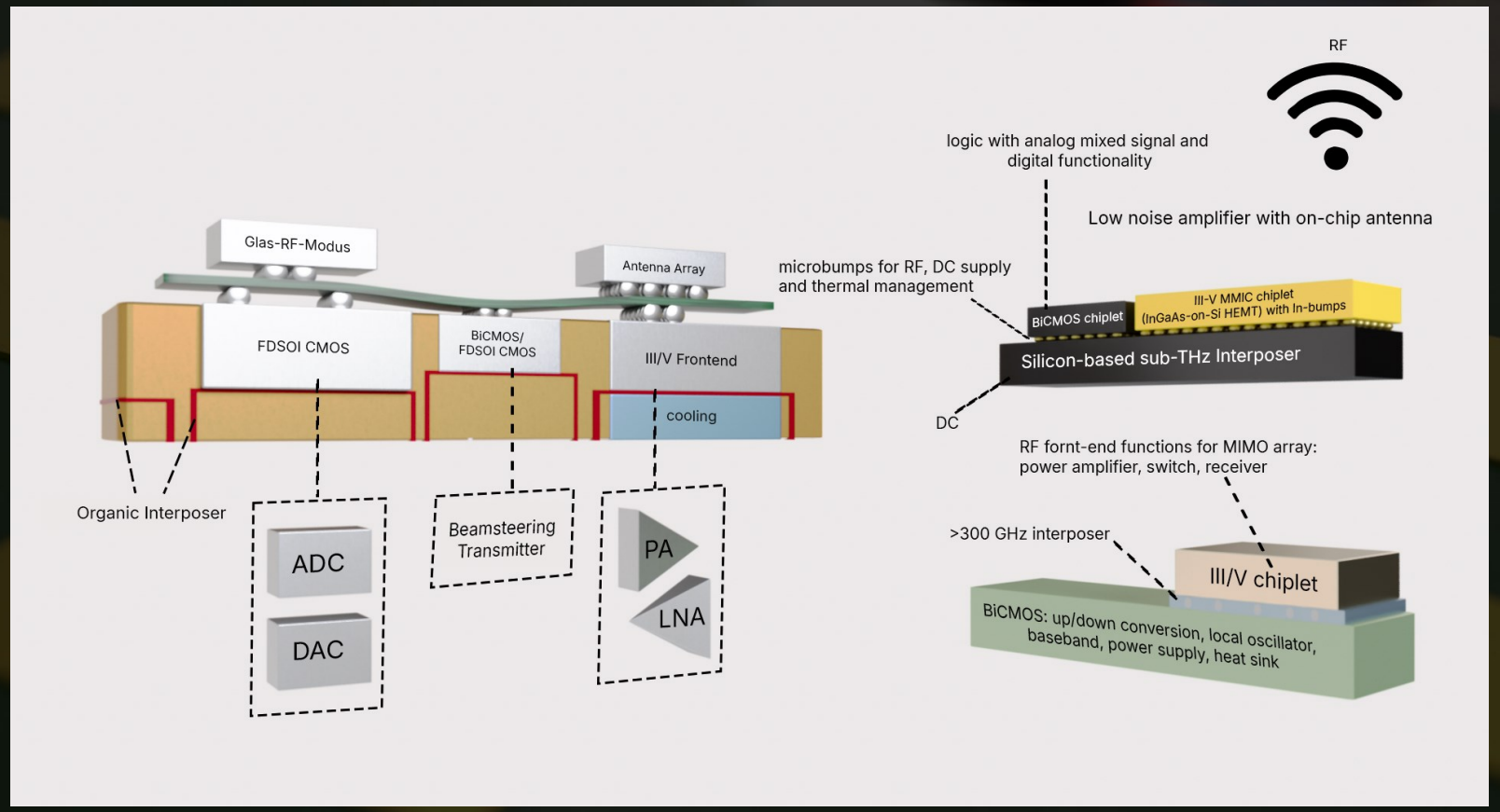

Integration of RF antennas as
an example for RF systems

3 RF subdemonstrators for different wavelengths



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3 RF subdemonstrators for different wavelengths

Target

D-band transceiver with bipolar InP chiplet on a SiGe-BiCMOS chip for 6G

- H-band transceiver with an InGaAs-on-Si-HEMT chiplet and BiCMOS chiplet on a Si-based sub-THz carrier substrate
- D-band radar transceiver module using a BiCMOS radar chiplet and an RF glass interposer with deposited antenna structure

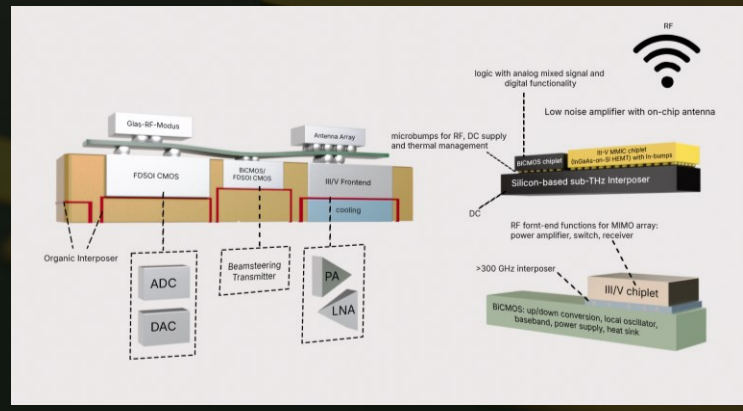
Innovations

- InP chiplets on SiGe-BiCMOS
- Fan-Out WLP embedding, which allows the integration of different semiconductor technologies
- RF-flex interposer technology

Impact

6G wireless communication:

- D-band transceiver
- H-band transceiver



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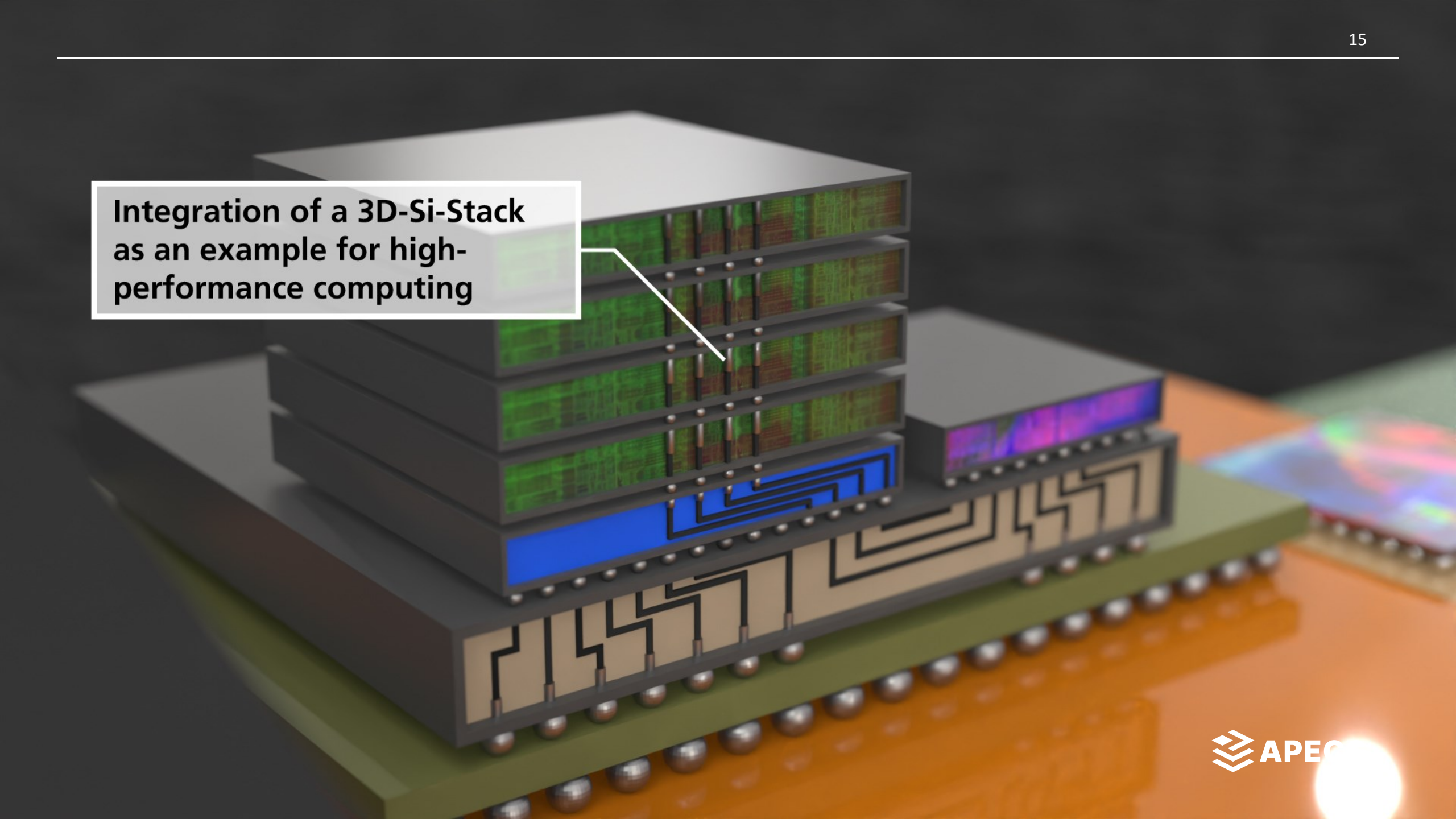
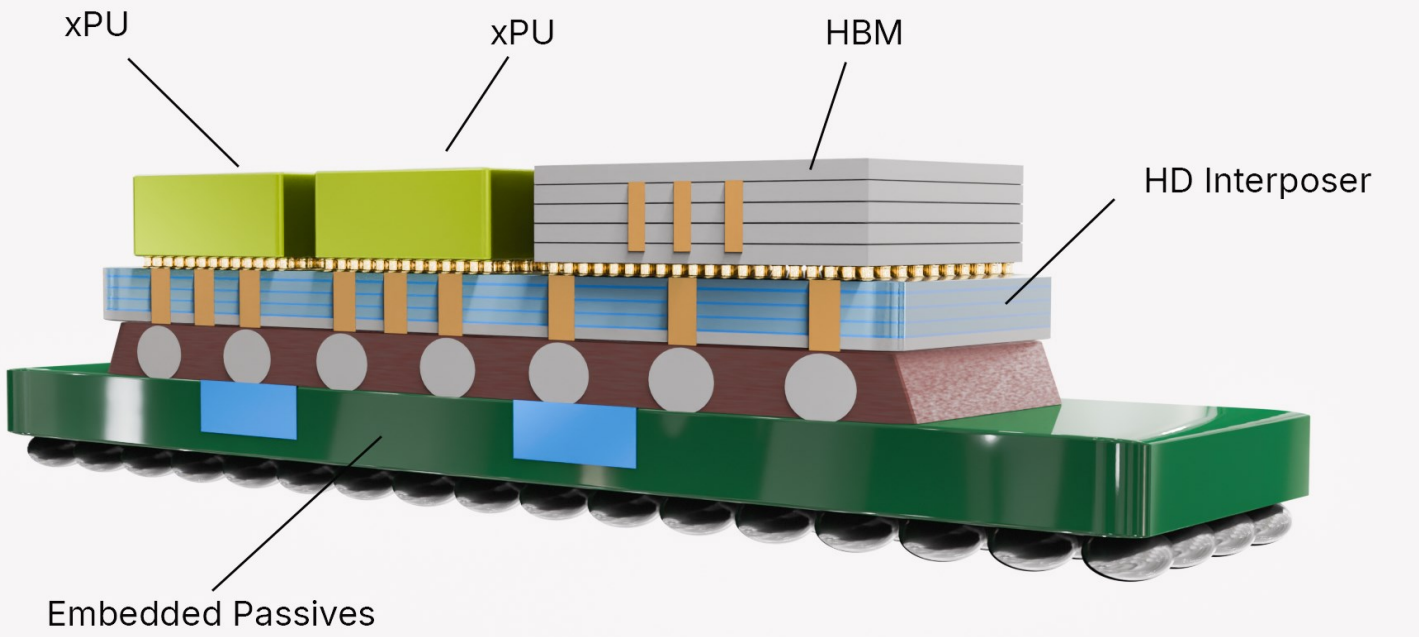

Integration of a 3D-Si-Stack as an example for high-performance computing

HPC Demonstrator



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HPC Demonstrator

Target

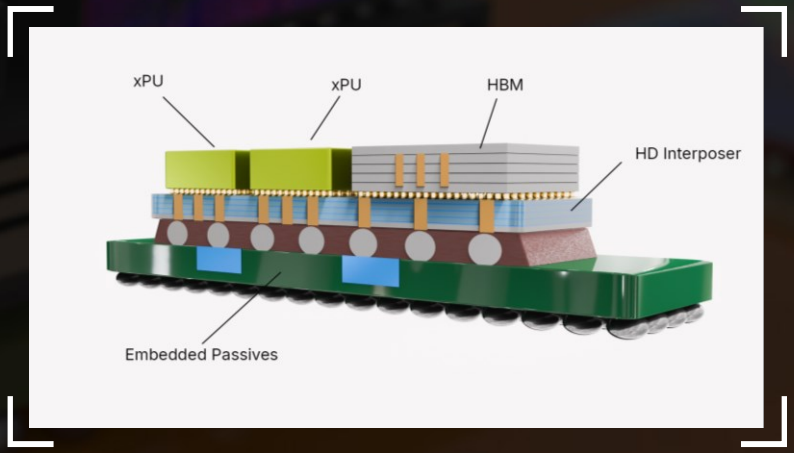
- STCO concept for HPC
- Silicon interposer(s) equipped with e.g. several compute- and accelerating-units and high bandwidth memory (HBM)

Impact

- HPC concepts for multiple applications
- Reduced development time by STCO

Innovations

- High speed, low-power and short distance die-to-die (D2D) data lanes between chiplets and memory stacks on Si/Glass and organics substrates
- Optimized signal and power integrity



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Key innovations of the APECS pilot line

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Key innovations of the APECS pilot line

1 Worldwide first **advanced automotive chiplet integration platform** (2.5D and 3D) for multiple core technologies (CMOS, Opto/RF) and non-electronic devices (MEMS, Opto, OLED), leveraging the innovations of advanced packaging

2 **Comprehensive end-to-end design flow and methodology** for chiplet-based advanced heterogeneous systems integration – Design-for-Performance, -Yield, -Power Efficiency, -Testability

3 Expansion of hetero-integration into **quasi-monolithic integration (QMI) for highest performance density** by leveraging Back-End-of-Line and Advanced Packaging capabilities

4 Prototyping of **high performance chiplet-based systems for specific needs of the European industries**, in particular, automotive, medical device and health care, sensors and advanced manufacturing industries

5 **Novel backend-of-line interfacing technology** for MEMS, opto/RF chips
(III/V RF chiplets with (Bi)CMOS for 100 GHz+ frequencies)

6 **Novel testing concepts and technologies** for function-, quality- and yield- optimization

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Workpackage: Chiplet Fabrication

Chiplet Interface Readiness for Heterogeneous Integration

Chiplets from external partners (RTOs, IDMs, Foundries,…)

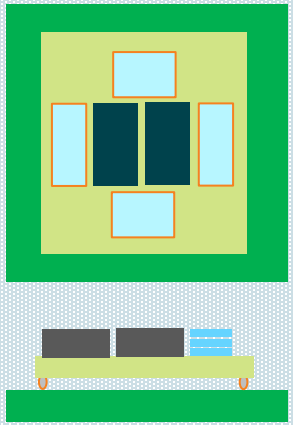
- Compute and Memory Integration
- Photonics Integration
- RF Integration
- QMI System Integration
- MEMS Integration

Characterization Test Reliability

Chiplet Integration Platforms

Functional Interposer

Rf/Photonic/Mems Interposer	Ultra High Density Interposer	Organic Interposer
200 mm Si/Glas	300 mm Si	Up to 600 mm



Toolbox for Functional Integration and Advanced Packaging

3D Stacks, Si-Bridge, µ-Bumps, Embedding, Assembly, …..

Wafer Level Packaging (WLP)

Based on thin film materials & equipment
100mm … up to 300 mm
CMOS – III / V - WBG wafers
2.5D / 3D integrated systems

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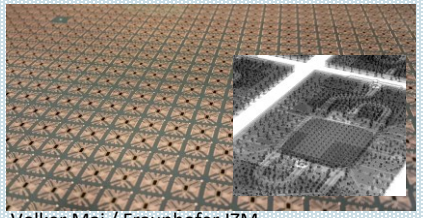
Panel Level Packaging (PLP)

Based on PCB materials & equipment
up to 610 x 456 mm²
CMOS - III / V - WBG dies (w/ bumping)
Packaged / embedded modules



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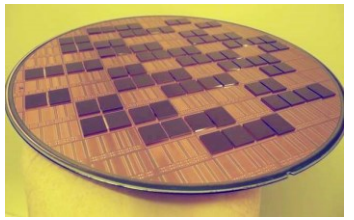
Characterization Test Reliability

APECS Demonstrators



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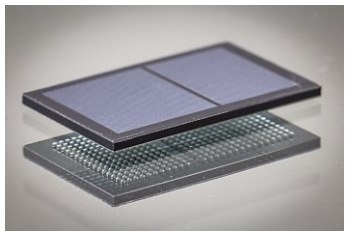
Demonstrators



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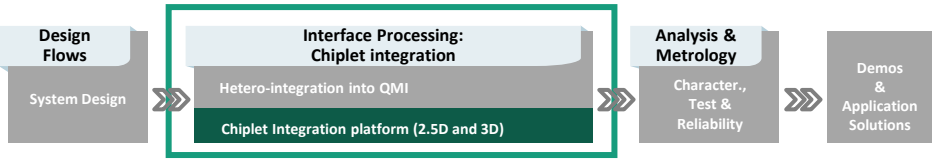
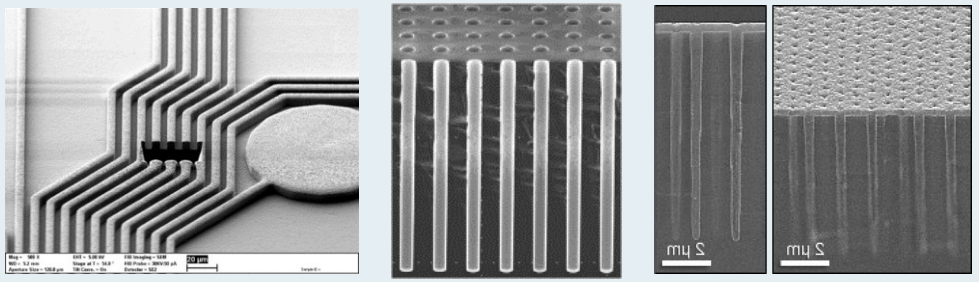
Chiplet Integration Platform

Functional Interposer



Target

- Anorganic Interposers for advanced CMOS on 300mm
- Multi-Functional Interposers for RF, Optoelectronics & MEMS*
- Passive Functionalities in Interposer
- Organic HD Interposers
- **Providing all required technologies for interposers based chiplet integration**



All pictures: Fraunhofer IZM

Innovations

- Sub-micron TSV´s, AR20:1,UHD Routing – incl. PostCMOS
- Glass, HR-Si, Ceramics with TxV´s and resp. routing, on 200mm
- IPDs, integrated cooling, LWGs, structural features
- Advanced HD substrates (5µm L/S)
- Laminates with embedded IC
- Panel Scale Interposers using FO processes

Impact

- Preparation for UHD Wafer Scale Integration, supporting QMI and Advanced Packaging
- Interposers serving Multi-Domain Systems (MEMS, Opto, RF, Sensing, *) for broad range of functionalities
- Critical functionalities integrated in a single process flow
- Module- and System Interfaces towards the applications

** Power Electronics is served but was excluded from the text due to potential interference with the PowerSemiconductor Pilot Line*

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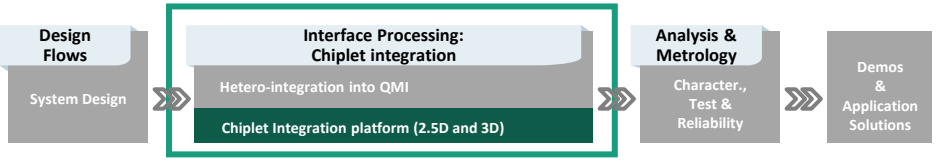
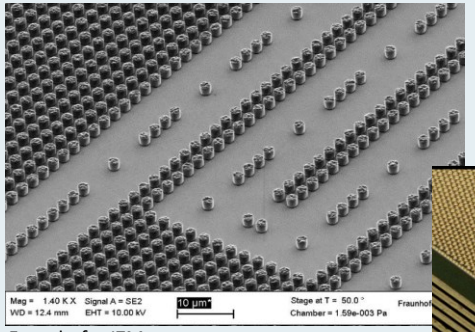


Chiplet Integration Platform

Functional Integration

Target

- 3D Stacking of advanced CMOS wafers and non-CMOS heterogenous/multimaterial wafers
- 2.5D Integration of chiplets onto interposer
- Preparation for chiplet interfaces
- Specific technologies for MEMS and sensor chiplets
- **Providing all technologies to realize heterogeneously integrated modules**



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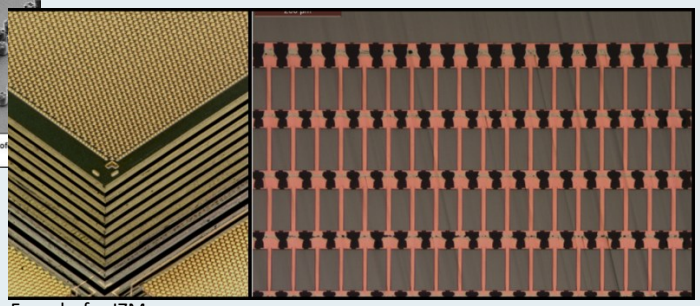

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Innovations

- High density Wafer2Wafer stacking with sub µm precision using hybrid bonding
- Stack-integration of specific functionalities for HIS providing hermeticity, capping
- Die2Wafer integration for heterogenous functionalities
- Chiplet interface adaption with RDLs, terminal metal & bumps

Impact

- Chiplet based module realization with functionalities from different domains
- Highest density integration of heterogenous chiplets
- Enabling STCO methodology throughout domains

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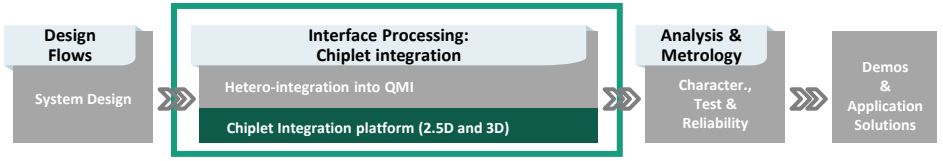
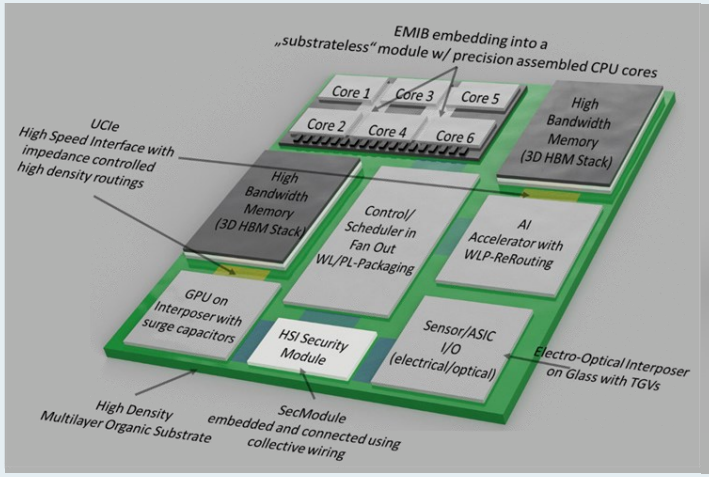


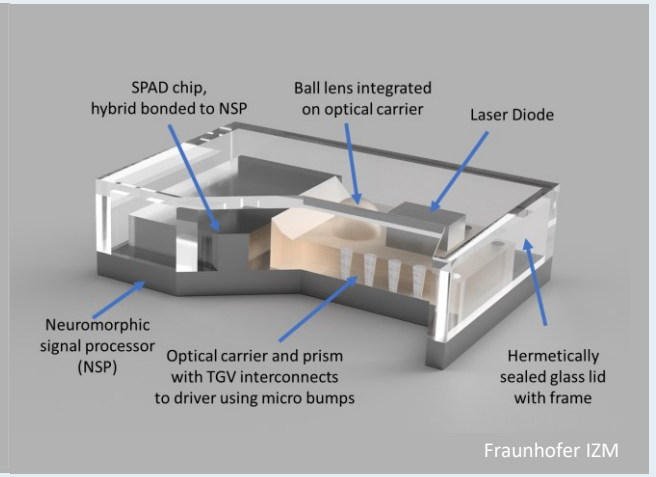
Chiplet Integration Platform

Advanced Packaging & Assembly

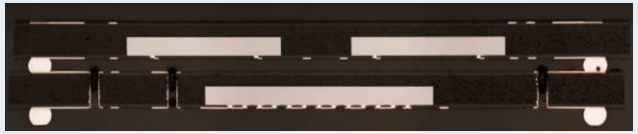
Target

- System scale assembly for Heterosystems with Modules and Subsystems
- Quality and Reliability assured functionalities at system level
- Novel integration concepts for 3D volumetric systems





Innovations



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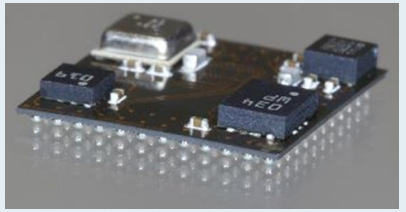
- High density, high speed, assembly on advanced substrates
- Reliable assembly for multi-layered heterogenous systems
- Embedded and fan out integration of systems
- Hybrid integration concept using embedding and fan out on panel scale
- Layer-by-Layer stacking for 3D volumetric system integration

Impact



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- Functional highly integrated for novel applications autonomous mobility, RF and Communication, Sensors, Power and Photonics
- Supporting STCO methodology

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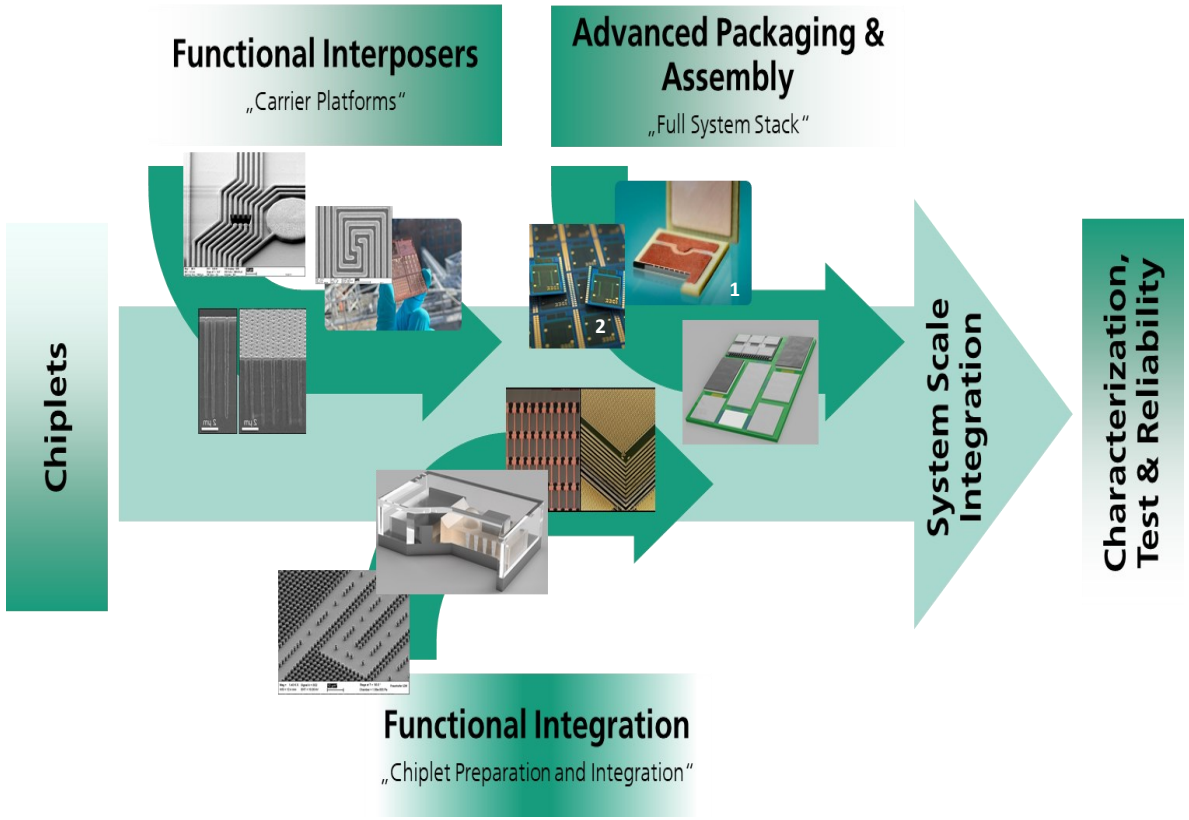
WP Chiplet Integration: Service Offer



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- **2.5 and 3D stack HD integration** of heterogeneous devices for silicon and non-silicon devices with µTSVs in the sub-µm range using microbumps and hybrid bonding innovations
- **MEMS and Sensor Integration** with 3D stacked chiplets up to 300 mm wafers for highly functional modules
- Scale-up of process implementation using **embedding technologies** into advanced substrates up to 600mm
- **Module and subsystem integration** HPC, NGC, Power-E, Sensors, UWBG & RF/Opto from chiplet to substrate
- **Scale-up of process** implementation for high-end chiplet architectures (3D, 2.5D) **up to 600 mm**
- **Open Access** for other Pilot Lines, RTO´s and industry to facilitate early adoption of new technologies & fast-track innovations

Coordinated by

Fraunhofer

Implemented by

Forschungsfabrik Mikroelektronik Deutschland

Pilot Line Project Partners

Fraunhofer MIKROELEKTRONIK

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Ministry of Economic Affairs and Employment of Finland

ANI Agência Nacional de Inovação

RÉPUBLIQUE FRANÇAISE Liberté Égalité Fraternité

Flanders State of the Art

Hellenic Republic Ministry of Development

Federal Ministry Republic of Austria Climate Action, Environment, Energy, Mobility, Innovation and Technology

Ministerio para la Transformación Digital y de la Función Pública

Business Finland

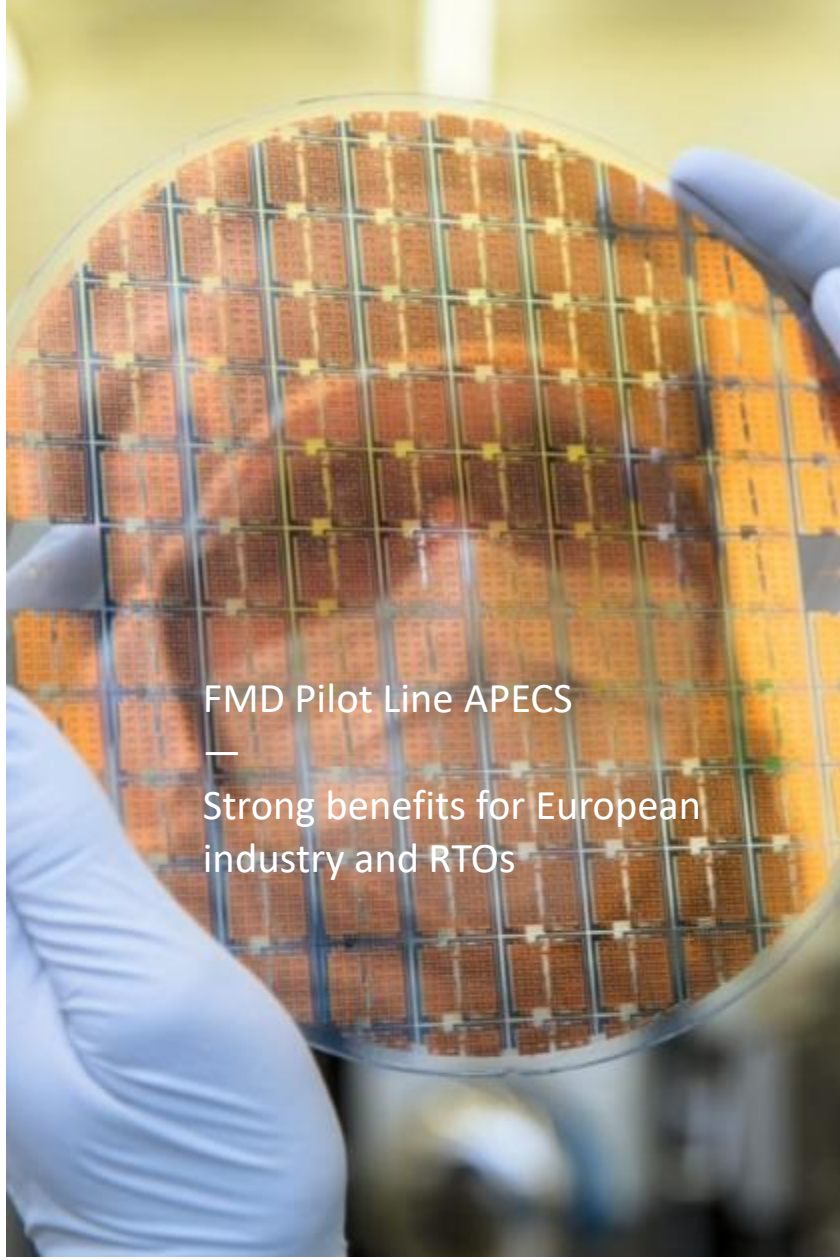
CCDR Norte

anr agence nationale de la recherche

FFG Promoting Innovation.

Executive Summary

1. Bundled access
   Offering innovative technologies via one interface
2. Complete value chains
   Offering both the complete value chain and individual components
3. Technology sovereignty
   APECS Pilot Line strengthens European technology sovereignty
   – also in cooperation with other pilot lines
4. Transfer of innovative technologies
   Small volume – scaling by industry



Thanks for Your Attention

Contact

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Fraunhofer Institute for Reliability and Microintegration IZM

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